

Form PTO 1449 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office					Atty. Docket No. IMPJ-0027C	Serial No.: Unassigned 10/814868
Information Disclosure Statement by Applicant					Applicant: Christopher J. Diorio et al.	
(Use several sheets if necessary)					Filed: 3/20/04 Group: Unassigned 3/20/04 2827	

U.S. Patent Documents

Init.		Document No.	Date	Name	Class	Subclass	Filing Date
SM	A	5,761,121	6/2/1998	Chang	365	185.14	10/31/1996
SM	B	5,825,063	10/20/1998	Diorio et al.	257	316	7/26/1996
SM	C	5,875,126	2/23/1999	Minch et al.	365	185.01	9/26/1996
SM	D	5,898,613	4/27/1999	Diorio et al.	365	185.03	6/25/1997
SM	E	5,914,894	6/22/1999	Diorio et al.	365	185.03	6/1/1998
SM	F	5,986,927	11/16/1999	Minch et al.	365	185.01	11/10/1998
SM	G	5,990,512	11/23/1999	Diorio et al.	257	314	4/22/1997
SM	H	6,125,053	9/26/2000	Diorio et al.	365	185.03	11/30/1998
SM	I	6,144,581	11/7/2000	Diorio et al.	365	185.03	11/30/1998
SM	J	6,222,765	4/24/2001	Nojima	365	185.08	2/18/2000
SM	K	6,452,835	9/17/2002	Diorio et al.	365	185.03	10/27/2000
SM	L	6,477,103	11/5/2002	Nguyen et al.	365	225.7	9/21/2001
SM	M	6,661,278	12/9/2003	Gilliland	327	536	7/8/2002
SM	N	6,664,909	12/16/2003	Hyde et al.	341	144	8/13/2001

Foreign Documents

Translation

Init.		Document No.	Date	Country	Class	Subclass	Yes	No

Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

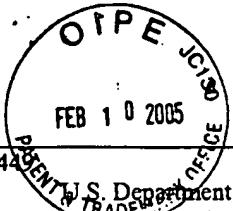
SM	O	Raszka, Jaroslav, et al., "Embedded Flash Memory for Security Applications in a 0.13µm CMOS Logic Process", IEEE 2004 International Solid-State Circuits Conference, February 16, 2004, pp. 46-47.

Examiner <i>/Son Mai/ (04/26/2006)</i>	Date Considered <i>04/26/2006</i>
Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with the next communication to applicant.	

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Init.		Document No.	Date	Name	Class	Subclass	Filing Date
SM	P	2003/0206437	11/6/2003	Diorio et al.	365	185.03	7/9/2002
SM	Q	2004/0004861	1/8/2004	Srinivas et al.	365	185.21	7/5/2002
SM	R	2004/002/1166	2/5/2004	Hyde et al.	257	314	1/31/2003
SM	S	2004/0037127	2/26/2004	Lindhorst et al.	365	202	5/12/2003
SM	T	2004/0052113 /	3/18/2004	Diorio et al.	365	185.21	9/16/2002
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Information Disclosure Statement by Applicant (Use several sheets if necessary)					Applicant: Christopher J. Diorio et al.			
					Filed: March 30, 2004	Group: 2827 2010		
U.S. Patent Documents								
Init.		Document No.	Date	Name	Class	Subclass	Filing Date	
SM	A	6,320,788	11/20/2001	Sansbury et al.				
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								Translation
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SM	B	Carley, L. Richard, "Trimming Analog Circuits Using Floating-Gate Analog MOS Memory", IEEE Journal of Solid-State Circuits, Vol. 24, No. 6, pp. 1569-1575, December 1989.						
SM	C	Partial International Search for International Application No. PCT/US03/31792, date mailed April 2, 2004.						
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Page 1 of 1

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<p>Information Disclosure Statement by Applicant</p> <p>(Use several sheets if necessary)</p>	<p>Applicant: Christopher J. Diorio et al.</p>	
	<p>Filed: March 30, 2004</p>	<p>Group: 2010 2827</p>

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SM	L	International Search Report, Application No.: PCT/US 03/31792, date of mailing August 12, 2004.
SM	M	Witters, et al., "Analysis and Modeling of On-Chip High-Voltage Generator Circuits for Use in EEPROM Circuits", IEEE Journal of Solid-State Circuits, VOL. 24, No. 5, October 1989, pp. 1372-1380.

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Init.		Document No.	Date	Country	Class	Subclass	Yes	No
SM	F	0 326 883	8/9/1989	EP			X	
	G	0 336 500	3/30/1989	EP			X	
SM								
SM	H	0 756 379	1/29/1997	EP			X	

Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

SM	I	International Search Report for International Application No. PCT/US05/10434, date of mailing 9/13/05.
SM	J	International Search Report for International Application No. PCT/US2005/010432, date of mailing 9/27/05.
SM	K	International Search Report for International Application No. PCT/US2005/010431, date of mailing 9/27/05.

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SM	R	Declercq et al., "Design and Optimization of High-Voltage CMOS Devices Compatible With a Standard 5 V CMOS Technology", IEEE Custom Integrated Circuits Conference, 1993, pp. 24.6.1-24.6.4.
SM	S	Dickson, "On-Chip High-Voltage Generation in MNOS Integrated Circuits Using an Improved Voltage Multiplier Technique", IEEE Journal of Solid-State Circuits, Vol. SC-11, No. 3, June 1976, pp. 374-378.
SM	T	Invitation to Pay Additional Fees for PCT/US 03/31792 date of mailing April 2, 2004.

Examiner

/Son Mai/ (04/26/2006)

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